

design ideas

Edited by Bill Travis and Anne Watson Swager

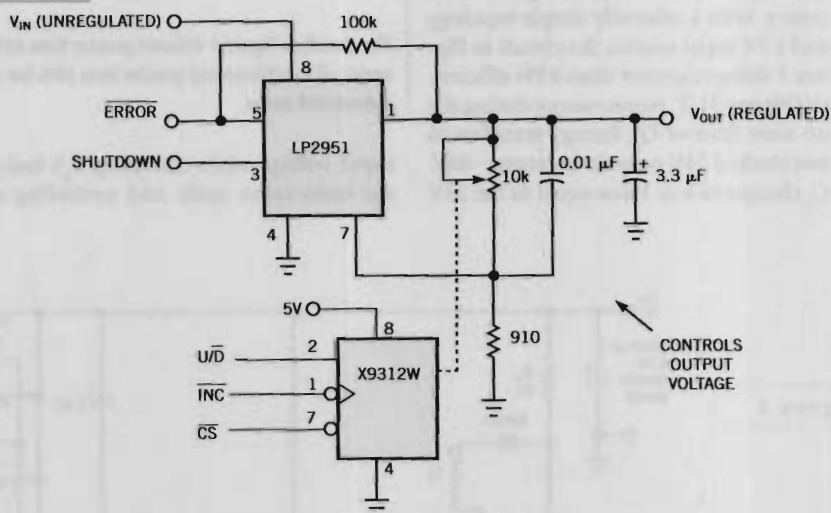
Voltage regulator goes digital

Chuck Wojslaw, Xicor Inc, Milpitas, CA

POWER CONSUMPTION AND failing batteries are key issues in battery-operated applica-

tions. Features in the new generation of series voltage regulators address these concerns. For example, National Semiconductor's LP2951 micropower voltage regulator provides a logic-level output signal indicating a low regulated output voltage; the IC also has a logic-level input to shut down the regulator to conserve power. These signals are digital; therefore, they are compatible with μ P-based systems. But what about the programming or controlling the regulator's output voltage? A mechanical potentiometer or selected resistors are not elegant solutions. You can complete the so-called computerization or digitizing of the voltage regulator by using a digitally controlled potentiometer to program the regulator's output voltage. The circuit in Figure 1 is a wide-range, computer-controlled voltage regulator with a nominal output voltage that varies from 1.235 to 14.8V. The regulator uses a Xicor XDCEP X9312W digitally controlled potentiometer that,

Figure 1



A digital potentiometer adds programmability to an ordinary series voltage regulator.

with its 100 steps, can program the regulator with a resolution of 0.136V per step. The output voltage is $1.235V(1 + kR/910\Omega)$, where k is a number from 0 to 1 and reflects the proportionate position of the wiper from one end of the pot (0) to the other end (1). R is the end-to-end resistance of the potentiometer.

The XDCEP's programming uses a three-wire bus. The potentiometer is configured as a two-terminal variable resistor. The regulator's Error output signal warns of a low output voltage; you can use it as a power-on reset. The logic-compatible Shutdown input signal allows you to switch the regulator on and off to conserve power. These signals, along with those you require to program the XDCEP, typically connect to the I/O port or the

μ P or μ C. The potentiometer adds variability to the regulator circuit; its digital controls, which are attached to a computer-controlled bus, provide programmability. For example, an automated closed-loop calibration procedure to program the regulator saves manufacturing test time. You can use the circuit as a bias supply; a voltage reference; or a programmable, high-output-current voltage source in test-and-measurement applications. (DI #2442).

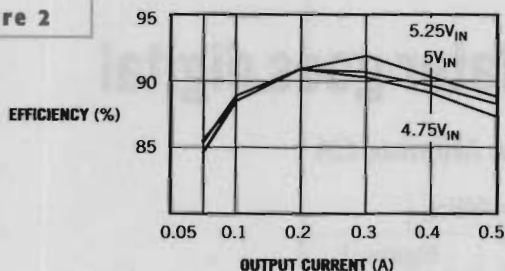
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Supply converts 5V to -48V

Kurk Mathews, Linear Technology Corp, Milpitas, CA

AS THE DEMAND for networking equipment grows, the need arises for a -48V supply that can power telecommunication lines. The circuit in Figure 1 delivers 24W at -48V from a 5V input. One of the biggest challenges in this design is choosing the input voltage. Although high-current, 5V sources are commonly available, lower input voltages generally mean high input currents with accompanying low efficiency. With a relatively simple topology and a 5V input source, the circuit in Figure 1 delivers greater than 85% efficiency (Figure 2). T_1 stores energy during the on-state time of Q_1 . Energy transfers to two stacked 24V outputs to create -48V. C_1 charges to a dc value equal to the 24V

Figure 2



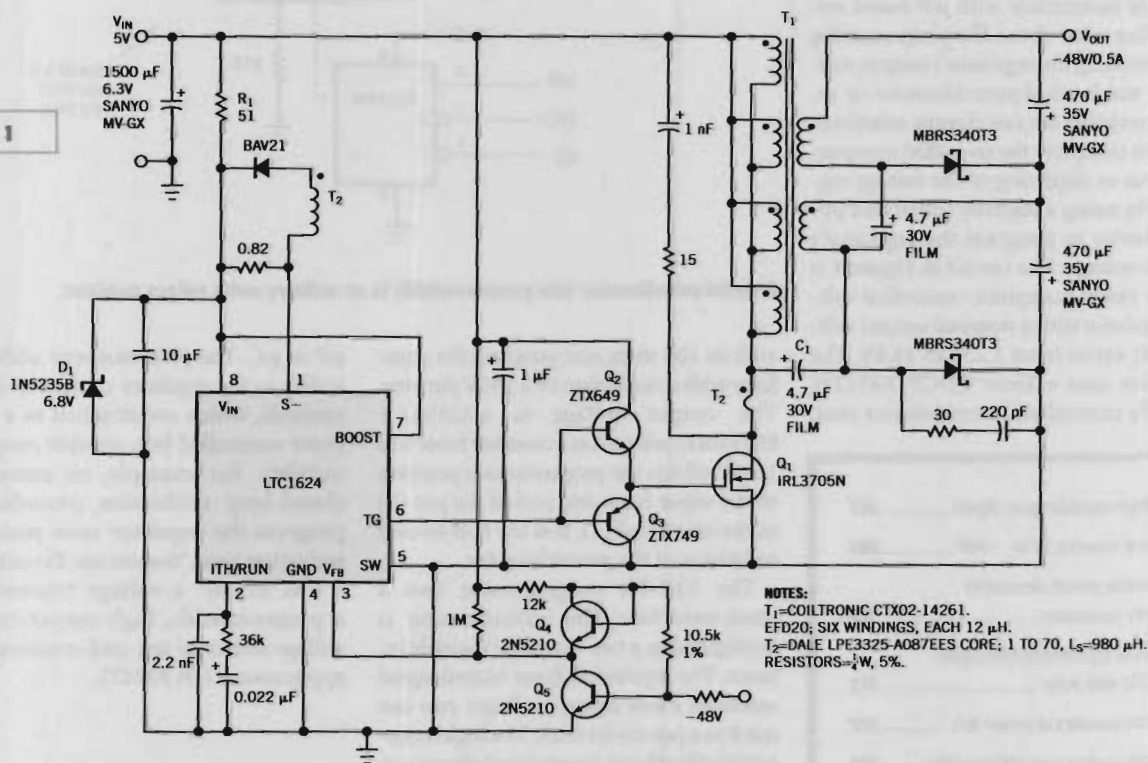
The circuit in Figure 1 delivers greater than 85% efficiency under all conditions and greater than 90% for much of its output-current range.

path for input current during Q_1 's off-state time. This operation results in continuous input current and thus reduces capacitor ripple-current requirements.

The reduced input ripple current, which is characteristic of this topology, demands sensing of the switch current rather than the input current. In this case, T_2 senses the switch current, eliminating 400 mW of resistor loss without using excessive board space (7×8 mm). Other additions improve the circuit's efficiency and per-

input voltage while clamping T_1 's leakage-inductance spike and providing a space (7×8 mm). Other additions improve the circuit's efficiency and per-

Figure 1



This circuit uses numerous tricks to boost efficiency to more than 85% in converting 5V to -48V.

formance. The LTC1624's Boost pin normally provides the internal output driver (the TG pin) with a 5.6V regulated supply, but TG produces only 4.2V with a 5V input. Bypassing the internal regulator by connecting the Boost and V_{IN} pins increases Q_1 's gate voltage, resulting in a gain of more than 3.2% in overall efficiency. R_1 and D_1 keep the Boost pin be-

low its 7.8V rating in the event of an input overvoltage condition. The addition of Q_2 and Q_3 provides an additional 5.5% of efficiency by speeding transitions and increasing gate voltage from 5 to 5.3V. This voltage peaking results from excess emitter current as Q_2 turns off after charging Q_1 's gate capacitance. Q_4 and Q_5 translate the -48V output to the 1.2V

that the feedback pin (V_{FB}) requires to regulate the output voltage. The LTC1624's switching frequency decreases with output voltage, thereby reducing input current during output short-circuit conditions. (DI #2440).

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 451

C routine speeds decimal-to-binary conversion

Giovanni Motta, Brandeis University, Waltham, MA

A PREVIOUS DESIGN IDEA ("Program provides integer-to-binary conversion," *EDN*, March 2, 1998, pg 110) describes a C/C++ function that provides integer-to-binary conversion. The function, named `cintbin/classicC`, implements a conversion in a straightforward way that defines decimal and binary numbers in terms of powers. Although this function can be useful for testing or educational purposes, its low efficiency precludes its use in embedded or other fast applications. The main source of inefficiency is the use of the `pow` C function, which requires linking the math library. By carefully rewriting the function and by directly accessing the binary representation of the integers in C, you can speed the conversion by as much as 58 times. The rewrite also results in more compact code, because linking the math library is unnecessary. **Listing 1** shows a simple calling program and two functions, `fast_d2b` and `fast_b2d`, that implement conversion between decimal and binary integer representations.

In `fast_d2b`, the main loop is a for loop, in which the variable, `i`, accesses the array, `c`, sequentially, from 0 to 31. At each iteration, `x`, the number to convert, right-shifts by `i` positions (the `>>` operator), and the routine extracts its least significant bit by masking `x` with the constant 1 (the `&` operator). The routine finally assigns the result to the `i`th term of the vector `c`. The symmetric `fast_b2d` function converts a binary number to its decimal

equivalent. The function performs the conversion through a sequence of left shifts and sums. To compare the performance of `fast_d2b` with

the function `classicC`, we ran several tests on two platforms, both running Unix-like OSs. We used the GNU C compiler (`gcc`) with and without turning on "aggressive optimization" (the `O3` flag). **Table 1** shows the time to convert the first 100 million integers. The Unix time command produces the running-time figure. `Fast_d2b` is 20 to 58 times faster

LISTING 1—DECIMAL-TO-BINARY CONVERSION IN C

```
/*
 * Fast decimal-to-binary conversions
 * Author: Giovanni Motta (gim@ieee.org)
 */
#include <stdio.h>
int c[32];

/*
 * Decimal to binary
 */
void fast_d2b(unsigned long x, int * c) {
    int i;

    for(i=0; i<32; i++)
        *c++ = (x >> i) & 0x1;
}

/*
 * Binary to decimal
 */
void fast_b2d(unsigned long int * n, int * c) {
    int i = 32;

    *n = 0;
    while(i-->0) {
        *n <<= 1;
        *n += *(c+i);
    }
}

main() {
    int k;
    unsigned long int x, y;

    printf("\nEnter an integer number");
    printf("\n smaller than 4,294,967,296 : ");
    scanf("%lu", &x);
    printf("\nCalling fast_d2b for ");
    printf("\ndecimal to binary conversion :\n");
    fast_d2b(x, c);
    printf(" Bin # = ");
    for (k=31; k>=0; k--)
        printf(" %d", c[k]);
    printf("\n\nCalling fast_b2d for ");
    printf("\nbinary to decimal conversion :\n");
    fast_b2d(&y, c);
    printf(" Dec # = %lu\n", y);
    return 0;
}
```

TABLE 1—SECONDS TO CONVERT 100 MILLION INTEGERS

	Irix (SGI Indy R5000)		Linux (PIII/500)	
	gcc	gcc-O3	gcc	gcc-O3
fast_d2b	476	160	80	28
classicC	9377	8542	2206	1672

than `classicC`. You can download **Listing 1** from *EDN*'s Web site. At the registered-user area, go into the Software Center and download the file from DI-SIG #2444. (DI #2443).

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 452

Resistor implements half-duplex RS-232 with echo

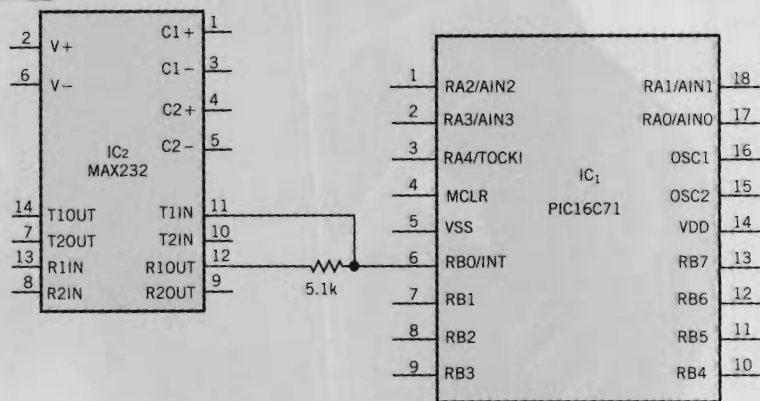
Matt Bennett, Austin, TX

A PREVIOUS DESIGN IDEA ("Single μ C pin makes half-duplex RS-232," *EDN*, Aug 5, 1999, pg

118) presented a way to implement half-duplex RS-232 communications without echo. Sometimes, an echo is desirable in a μ C application. You can obtain the echo by using a single resistor (**Figure 1**). You insert a 5.1-k Ω resistor between the transmit and receive pins on the RS-232 driver (such as a MAX232). The I/O pin on the μ C (RB0 on 14-bit PIC μ Cs) connects directly to the transmit gate on the RS-232 driver. This technique is useful for implementing a user interface on a Microchip PIC for applications in which you communicate to the PIC via a terminal or a terminal-emulation program. Full duplex is unnecessary with a user interface based on user-issued commands and μ C responses, when the μ C generates no spontaneous data that would mask the user-issued commands. The character echo is useful in determining whether the device is powered up and the RS-232 receiver is active, but an echo alone does not tell you whether the μ C is active; the μ C must send data.

When the μ C is in receive mode, it makes the input pin a high-impedance

Figure 1



The addition of a single resistor provides an echo in RS-232 half-duplex communications.

input. All RS-232 data sent to the μ C is immediately retransmitted via the resistor that connects the receiver to the transmitter. Because the input has high impedance, the μ C is essentially just monitoring the traffic on the RS-232 line. When the μ C must send serial information, the μ C converts its I/O pin to a low-impedance driver. Anything now sent to the μ C shunts to ground or V_{CC} (depending on the μ C's output state)

through the resistor and the μ C's driver. The μ C ignores data sent to it. The μ C now directly sends data down the serial line. The μ C must immediately change the serial line back to high-impedance mode after transmitting or risk data loss. (DI #2445).

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 453

Circuit monitors ac-power loss

Dennis Eichenberg, Parma Heights, OH

THE CIRCUIT IN **Figure 1** provides a simple, nonvolatile means of monitoring critical ac-power failures. Monitoring the power is important in such systems as heating and refrigeration, in which damage can occur if the ac power goes down for an extended period. The circuit in **Figure 1** requires little power from the ac-power system. The quiescent battery current of approximately 5 μ A

provides long battery life in this application. The optocoupler consists of a neon lamp and a photocell. When the ac-power system is active, the neon lamp lights via current-limiting resistor R_1 . A neon lamp is ideal for this application because of its low power drain. The resistance of the photocell in the optocoupler is low when the cell is illuminated and high when it's unilluminated. R_2 serves as a

current-limiting resistor for the photocell.

IC_{1A} of the quad two-input NAND-gate Schmitt trigger serves as a buffer for the optocoupler. The output of IC_{1A} is normally high when the ac power is present and goes low when a power failure occurs. IC_{1B} is configured as a negative-edge-triggered, half-monostable multivibrator. It produces a positive pulse with

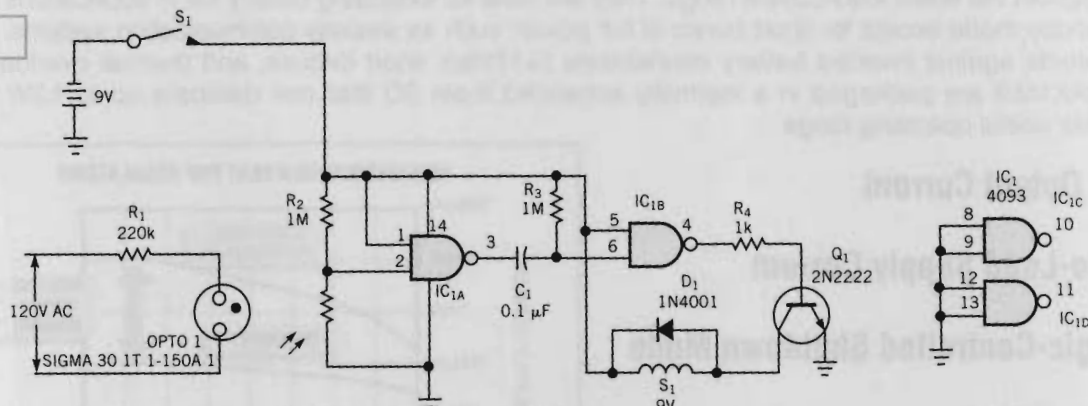
a width of approximately $0.8R_3C_1$, or approximately 0.8 sec, whenever the ac power goes down. The output pulse drives transistor Q_1 via the current-limiting resistor, R_4 , to activate solenoid S_1 .

D_1 is a flyback diode to protect Q_1 from the inductive spike S_1 generates when it becomes deactivated. You can use S_1 to trigger a flag or to provide a similar visual alarm. The flag remains in position

until you manually reset it to prepare the circuit for the next power failure. (DI #2446).

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Figure 1



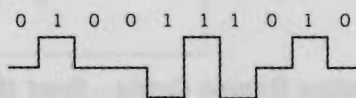
This circuit sets a flag or triggers a visual alarm when the ac-power line fails.

RF transmitter uses AMI encoding

Paul Sofianos, Motorola, Tempe, AZ

ALTHOUGH ALTERNATE-MARK-INVERSION (AMI) encoding is well-suited for direct-conversion FM transmission, designers often overlook the technique. AMI, a three-phase, synchronous-encoding technique, uses bipolar pulses to represent logic ones and no signal to represent logic zeros (Figure 1). Direct-conversion FM transmission, in which data directly modulates a carrier, is also known as frequency-shift-keying (FSK) modulation. For higher frequency transmissions, a PLL usually synthesizes the carrier from a crystal reference. This type of RF transmission requires the dc voltage of the modulating signal to be 0V; otherwise, the PLL tends to "track out" the transmitted data. FSK transmission usually uses the familiar Manchester-encoding method. However,

Figure 1



AMI encoding uses a pulse of either polarity to denote a logic one and a 0V level to denote a logic zero.

Manchester encoding requires twice the bandwidth of AMI encoding and usually requires the addition of preamble and postamble bits to allow the receiver to determine the center of the data bit for decoding. AMI suffers from none of these

disadvantages; however, it has a drawback: A long string of zeros produces no transitions in the data stream. To address this drawback, high-density bipolar 3 (HDB3) encoding is available.

The circuit in Figure 2 shows a 16-channel, AMI-encoded RF transmitter for data rates as high as 28.8 kbps. The circuit operates in the unlicensed (FCC Part 15) 902- to 928-MHz industrial, scientific, and medical (ISM) band and is reliable for open-field distances as long as 1000 ft. You can easily modify it to sustain higher or lower data rates. IC_1 , IC_2 , R_1 , and R_2 perform the AMI encoding. IC_{1A} , a simple D flip-flop, controls the high-impedance state on Pin 13 of IC_2 . IC_{1B} alternates the data presented to IC_2 whenever the previous data is a logic one. This data has a slight delay to avoid

glitches in the output waveform. R_1 and R_2 set the high-impedance voltage to $\frac{1}{2}V_{CC}$. R_2 adjusts the peak deviation of the transmitted RF signal from IC_3 , nominally set at 50 kHz. C_1 and R_2 constitute a lowpass filter with corner frequency set to attenuate the data at frequencies above the third harmonic.

IC_3 is a low-power, integrated RF transmitter (Motorola, www.motorola.com) targeting ISM applications. Its voltage-controlled oscillator is a parallel-resonant Colpitts type. The varactor diode, D_1 , controls the modulation, and D_2 sets the center frequency. The modulation, D_1 , is set to approximately 60 kHz/V, and the frequency adjustment, D_2 , is set to 7

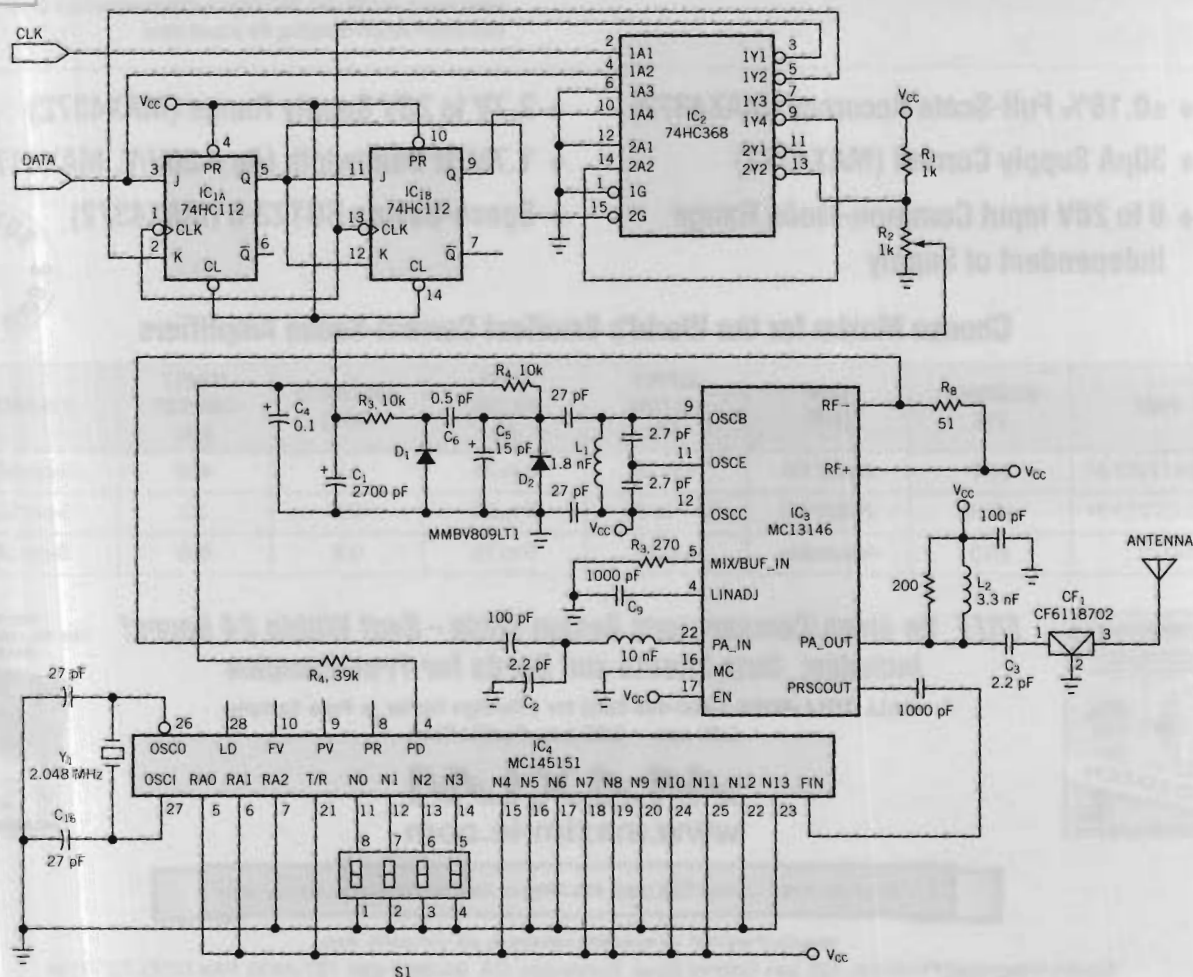
MHz/V. The mixer of the IC serves as a buffer; you can adjust R_3 for desired output power. C_2/L_1 and C_3/L_2 conjugately match the source-to-load impedances. These values can vary, depending on the parasitics of your layout. CF_1 (TDK Corp, www.tdk.com) provides final filtering of the output before transmission. IC_4 synthesizes the desired carrier frequency. The IC internally divides by 512 the frequency that crystal Y_1 establishes. With Pin 16 of IC_3 tied low, the synthesized frequency is $f_{OUT} = (2.048 \text{ MHz}/512) \cdot 65 \cdot N$, where N represents the digital value present on the N bus of IC_4 .

As illustrated, N can vary from 3472 to 3487, yielding 16 discrete output chan-

nels from 902.72 to 906.62 MHz in 260-kHz steps. R_4 and C_4 form a lowpass filter with corner frequency set to a value substantially lower than the internal reference frequency of the synthesizer or the data stream, whichever is lower. As with any RF design, you should give careful consideration to parts placement and shielding. You should also apply generous decoupling. If desired, you can hold Pin 17 of IC_3 at logic zero for low-power-disabled operation. (DI #2429).

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 455

Figure 2

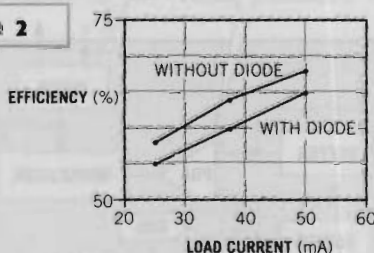


High-voltage regulator is 100%-surface-mountable

Tom Gross, Linear Technology Corp, Milpitas, CA

IT CAN BE DIFFICULT to generate a high-voltage supply from a medium-voltage input, especially if you need a surface-mount design. It is difficult to find surface-mount components with the necessary specs, especially the transformer and power switches. High-voltage surface-mount capacitors can also be hard to locate. The circuit in **Figure 1** generates 100V from 25V. The circuit is a typical flyback regulator that uses a couple of well-established circuit techniques to handle the high voltage. The first technique is to insert an n-channel MOSFET (Si4480) in series with IC₁'s internal power transistor. The cascoded FET stands off the large switch voltage that arises when the switch turns off. The large switch voltage represents the input voltage summed with the reflected output voltage of the transformer's primary. Using the cascode FET not only increases the effective switch-voltage capability, but also eliminates the

Figure 2



Bootstrapping the IC switch voltage to the input in the circuit of Figure 1 improves efficiency by about 3%.

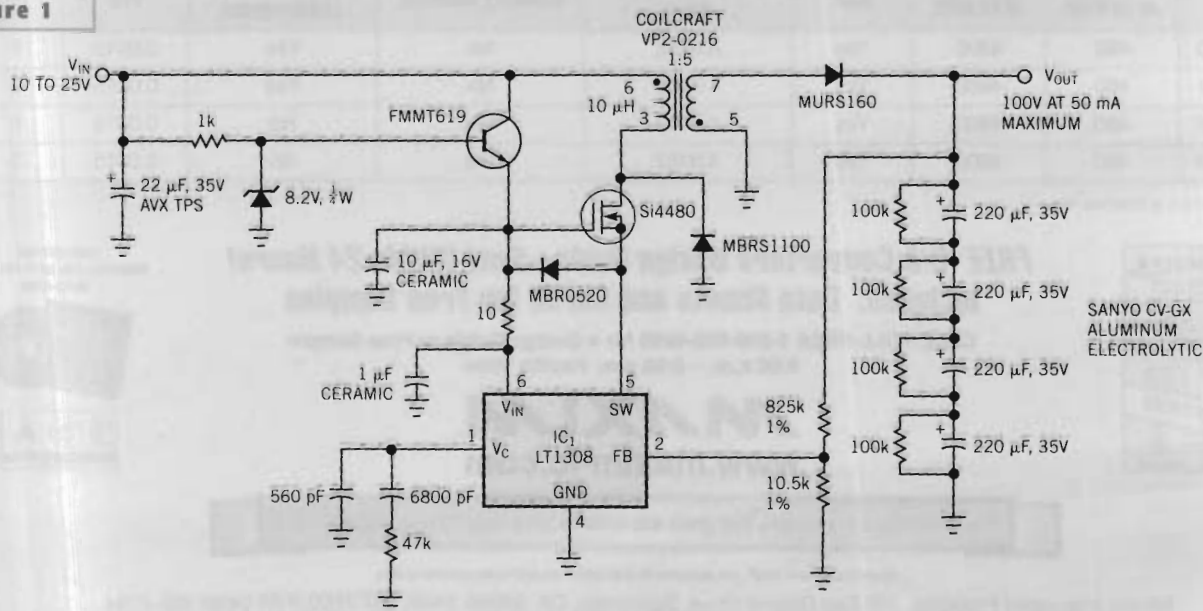
need for a snubber circuit across the primary of the transformer.

Of course, the FET actively turns on when the source goes low. But simply using the input voltage to supply the gate voltage doesn't work, because the maximum input voltage (25V) exceeds the maximum $\pm 20V$ limit of the MOSFET's gate-to-source voltage. Therefore, the cir-

cuit uses an emitter follower to supply a constant voltage to the gate of the MOSFET. A 1-k Ω resistor delivers bias current to an 8.2V zener diode at the base of the npn transistor and provides base current to the npn. This arrangement sets the npn's emitter and the FET gate connected to it at 7.5V—more than enough voltage for a logic-level FET. The input to IC₁ also connects to the emitter through an RC filter. A convenient feature of this circuit is that the IC switch voltage feeds back through the diode to the input (bootstrapping). This connection allows for a small boost in efficiency, negating the loss of efficiency from using a cascoding FET and the emitter-follower circuit. **Figure 2** shows the efficiency of the regulator with and without the bootstrapped diode at different load currents. (DI #2439).

TO VOTE FOR THIS DESIGN,
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Figure 1



This bootstrapped high-voltage regulator uses all surface-mount components.